What is claimed is:

1. A non-volatile memory device comprising:
a non-volatile memory array;
a buffer memory;
a synchronous memory interface; and
a controller coupled to the non-volatile memory array, the buffer memory, and the synchronous memory interface, wherein the controller is adapted to interface to and manage the non-volatile memory array and buffer memory and to present the non-volatile memory device as a synchronous memory device through the synchronous memory interface.

2. The non-volatile memory device of claim 1, wherein the controller is adapted to buffer data accesses to the non-volatile memory array in the buffer memory.

3. The non-volatile memory device of claim 2, wherein the controller is adapted to buffer read data accesses to the non-volatile memory array in the buffer memory.

4. The non-volatile memory device of claim 3, wherein the controller is adapted to buffer read data accesses to the non-volatile memory array in the buffer memory in a least recently used manner.

5. The non-volatile memory device of claim 3, wherein the controller is adapted to buffer a current data block to the non-volatile memory array in the buffer memory while accessing a sequentially following data block from the non-volatile memory array.

6. The non-volatile memory device of claim 2, wherein the controller is adapted to buffer write data accesses to the non-volatile memory array in the buffer memory.

7. The non-volatile memory device of claim 6, wherein the controller is adapted to buffer write data accesses to the non-volatile memory array in the buffer memory in a write-through manner.

8. The non-volatile memory device of claim 6, wherein the non-volatile memory device is adapted to indicate when the non-volatile memory device is busy by changing the status of one of an external "ready/busy" pin and a status register.

9. The non-volatile memory device of claim 8, wherein the non-volatile memory device is adapted to indicate when the buffer memory is full during a write access by asserting one of an external "ready/busy" pin and a status register.

10. The non-volatile memory device of claim 1, wherein the non-volatile memory device is one of a NAND architecture Flash, a NOR architecture Flash, EEPROM, Polymer Memory, Ferroelectric Random Access Memory (FeRAM), Ovionics Unified Memory (OUM), Magnetoresistive Random Access Memory (MRAM), Molecular Memory, and Carbon Nanotube Memory.

11. The non-volatile memory device of claim 1, wherein the synchronous interface is one of a SDRAM interface, a DDR interface, a DDR2 interface, GDDR interface, GDDR2 interface, and RDRAM interface.

12. The non-volatile memory device of claim 1, wherein the non-volatile memory is adapted to present as one of a compatible read/write capable SDRAM device, a DDR device, a DDR2 device, a GDDR device, a GDDR2 device, and a RDRAM device.

13. The non-volatile memory device of claim 1, wherein the non-volatile memory device is a BIOS boot memory.

14. The non-volatile memory device of claim 1, wherein the non-volatile memory is adapted to have a burst data access mode.

15. The non-volatile memory device of claim 1, wherein the controller is adapted to generate and evaluate ECC data.

16. The non-volatile memory device of claim 15, wherein the controller is adapted to generate and evaluate ECC data in an ECC hardware circuit.

17. The non-volatile memory device of claim 1, further comprising:
a DRAM memory array coupled to the controller.

18. The non-volatile memory device of claim 17, wherein the controller is adapted to selectively couple the DRAM memory array to the synchronous memory interface.

19. The non-volatile memory device of claim 17, wherein the controller is adapted to selectively copy data from the non-volatile memory array and remap addresses of one or more DRAM memory array section to the synchronous memory interface to operate as "shadow" memory.

20. The non-volatile memory device of claim 17, wherein the controller is adapted to operate the DRAM memory array as an extended read and/or write data buffer memory.

21. The non-volatile memory device of claim 17, wherein the controller is adapted to operate the DRAM memory array as "scratch pad" memory.

22. A NAND architecture Flash memory device comprising:
a NAND architecture Flash memory array;
a buffer memory;

a synchronous memory interface; and

a controller coupled to the NAND architecture Flash memory array, the buffer memory, and the synchronous memory interface, wherein the controller is adapted to interface to and manage the NAND architecture Flash memory array and to portray the NAND architecture Flash memory device as a synchronous memory device through the synchronous memory interface.

23. The NAND architecture Flash memory device of claim 22, wherein the controller is adapted to buffer data accesses to the NAND architecture Flash memory array in the buffer memory.

24. The NAND architecture Flash memory device of claim 23, wherein the controller is adapted to buffer read data accesses to the NAND architecture Flash memory array in the buffer memory.

25. The NAND architecture Flash memory device of claim 24, wherein the controller is adapted to buffer read data accesses to the NAND architecture Flash memory array in the buffer memory in a least recently used manner.

26. The NAND architecture Flash memory device of claim 23, wherein the controller is adapted to buffer write data accesses to the NAND architecture Flash memory array in the buffer memory.

27. A non-volatile memory subsystem comprising:

one or more non-volatile memory devices;

a buffer memory;

a synchronous memory interface; and

a controller coupled to the one or more non-volatile memory devices, the buffer memory, and the synchronous memory interface, wherein the controller is adapted to interface to and manage the non-volatile memory devices and to present the non-volatile memory devices as a synchronous memory device

through the synchronous memory interface.

28. The non-volatile memory subsystem of claim 27, wherein at least one of the one or more non-volatile memory devices is one of a NAND architecture Flash, a NOR architecture Flash, EEPROM, Polymer Memory, Ferroelectric Random Access Memory (FeRAM), Ovionics Unified Memory (OUM), Magnetoresistive Random Access Memory (MRAM), Molecular Memory, and Carbon Nanotube Memory.

29. The non-volatile memory subsystem of claim 27, wherein the controller is adapted to buffer data accesses to the one or more non-volatile memory devices in the buffer memory.

30. The non-volatile memory subsystem of claim 29, wherein the controller is adapted to buffer read data accesses to the one or more non-volatile memory devices in the buffer memory.

31. The non-volatile memory subsystem of claim 29, wherein the controller is adapted to buffer write data accesses to the one or more non-volatile memory devices in the buffer memory.

32. The non-volatile memory subsystem of claim 29, wherein the non-volatile memory subsystem is adapted to indicate when the non-volatile memory subsystem is busy by changing the status of one of an external "ready/busy" pin and a status register.

33. The non-volatile memory subsystem of claim 31, wherein the non-volatile memory subsystem is adapted to indicate when the buffer memory is full during a write access by asserting one of an external "busy" pin and a status register.

34. The non-volatile memory subsystem of claim 27, wherein the synchronous interface is one of a SDRAM interface, a DDR interface, a DDR2 interface, GDDR interface, GDDR2 interface, and RDRAM interface.

35. The non-volatile memory subsystem of claim 27, wherein the non-volatile memory subsystem is adapted to present as one of a compatible read/write capable SDRAM device, a DDR device, a DDR2 device, a GDDR device, a GDDR2 device, and a RDRAM device.

36. The non-volatile memory subsystem of claim 27, wherein the non-volatile memory subsystem is adapted to have a burst data access mode.

37. The non-volatile memory subsystem of claim 27, wherein the controller is adapted to generate and evaluate ECC data.

38. The non-volatile memory subsystem of claim 37, wherein the controller further comprises:
an ECC hardware circuit coupled to the one or more non-volatile memory devices.

39. The non-volatile memory subsystem of claim 27, further comprising:
one or more synchronous DRAM memory devices coupled to the controller.

40. The non-volatile memory subsystem of claim 39, wherein the controller is adapted to selectively couple the one or more synchronous DRAM memory devices to the synchronous memory interface.

41. The non-volatile memory subsystem of claim 39, wherein the controller is adapted to selectively copy data from the one or more non-volatile memory devices and remap addresses of the one or more synchronous DRAM memory devices to the synchronous memory interface to operate as "shadow" memory.

42. The non-volatile memory subsystem of claim 39, wherein the controller is adapted to operate the one or more synchronous DRAM memory devices as an extended read and/or write data buffer memory.

43. The non-volatile memory subsystem of claim 39, wherein the controller is adapted to operate the one or more synchronous DRAM memory devices as "scratch pad" memory.

44. The non-volatile memory subsystem of claim 39, wherein the one or more synchronous DRAM memory devices are one of SDRAM device, a DDR device, a DDR2 device, a GDDR device, a GDDR2 device, and a RDRAM device.

45. A system comprising:

a host; and

one or more non-volatile memory devices coupled to the host, wherein each of the one or more non-volatile memory devices comprises,

a non-volatile memory array;

a buffer memory;

a synchronous memory interface; and

a controller coupled to the non-volatile memory array, the buffer memory, and the synchronous memory interface, wherein the controller is adapted to interface to and manage the non-volatile memory array and to present the non-volatile memory device as a synchronous memory device through the synchronous memory interface.

46. The system of claim 45, wherein at least one of the one or more non-volatile memory devices is one of a NAND architecture Flash, a NOR architecture Flash, EEPROM, Polymer Memory, Ferroelectric Random Access Memory (FeRAM),

Ovionics Unified Memory (OUM), Magnetoresistive Random Access Memory (MRAM), Molecular Memory, and Carbon Nanotube Memory.

47. The system of claim 45, wherein the controller of each non-volatile memory device is adapted to buffer data accesses to the non-volatile memory array in the buffer memory.

48. The system of claim 47, wherein the controller is adapted to buffer read data accesses to the non-volatile memory array in the buffer memory.

49. The system of claim 47, wherein the controller is adapted to buffer write data accesses to the non-volatile memory array in the buffer memory.

50. The system of claim 47, wherein each non-volatile device is adapted to indicate when the non-volatile memory device is busy by changing the status of one of an external "ready/busy" pin and a status register.

51. The system of claim 49, wherein each non-volatile memory device is adapted to indicate when the buffer memory is full during a write access by changing the status of one of an external "ready/busy" pin and a status register.

52. The system of claim 45, wherein the synchronous interface of each non-volatile memory device is one of a SDRAM interface, a DDR interface, a DDR2 interface, GDDR interface, GDDR2 interface, and RDRAM interface.

53. The system of claim 45, wherein each non-volatile memory device is adapted to present as one of a compatible read/write capable SDRAM device, a compatible read/write capable DDR device, a compatible read/write capable DDR2 device, a compatible read/write capable GDDR device, a compatible read/write capable GDDR2 device, and a compatible read/write capable RDRAM device.

54. The system of claim 45, wherein at least one non-volatile memory device is a boot memory.

55. The system of claim 45, wherein each non-volatile memory device further comprises:
a DRAM memory array coupled to the controller.

56. The system of claim 55, wherein the controller is adapted to selectively couple the DRAM memory array to the synchronous memory interface.

57. The system of claim 55, wherein the controller is adapted to selectively copy data from the non-volatile memory array and remap addresses of one or more DRAM memory array section to the synchronous memory interface to operate as "shadow" memory.

58. The system of claim 55, wherein the controller is adapted to operate the DRAM memory array as an extended read and/or write data buffer memory.

59. The system of claim 55, wherein the controller is adapted to operate the DRAM memory array as "scratch pad" memory.

60. A method of operating a non-volatile memory device comprising:
managing the non-volatile memory device with an internal controller;
presenting the non-volatile memory device as a synchronous memory device through a synchronous memory interface; and
buffering data access requests received through the synchronous memory interface in an internal buffer memory.

61. The method of claim 60, wherein the non-volatile memory device is one of a NAND architecture Flash, a NOR architecture Flash, EEPROM, Polymer Memory, Ferroelectric Random Access Memory (FeRAM), Ovionics Unified Memory (OUM), Magnetoresistive Random Access Memory (MRAM), Molecular Memory, and Carbon Nanotube Memory.

62. The method of claim 60, wherein buffering data access requests received through the synchronous memory interface in an internal buffer memory further comprises buffering read data access requests in the internal buffer memory.

63. The method of claim 60, wherein presenting the non-volatile memory device as a synchronous memory device through a synchronous memory interface further comprises changing the status of one of an external "ready/busy" pin and a status register to indicate that the non-volatile memory device is busy.

64. The method of claim 60, wherein buffering data access requests received through the synchronous memory interface in an internal buffer memory further comprises changing the status of one of an external "ready/busy" pin and a status register to indicate that the non-volatile memory device is busy.

65. The method of claim 60, wherein buffering data access requests received through the synchronous memory interface in an internal buffer memory further comprises buffering write data access requests in the internal buffer memory.

66. The method of claim 65, wherein buffering write data access requests received through the synchronous memory interface in an internal buffer memory further comprises asserting one of an external "busy" pin and a status register to indicate that the buffer memory is full during a write access.

67. The method of claim 60, wherein presenting the non-volatile memory device as a synchronous memory device through a synchronous memory interface further comprises presenting one of a SDRAM device, a DDR device, a DDR2 device, a GDDR device, a GDDR2 device, and a RDRAM device.

68. The method of claim 67, wherein presenting one of a SDRAM device, a DDR device, a DDR2 device, a GDDR device, a GDDR2 device, and a RDRAM device further comprises presenting as one of a compatible read/write capable SDRAM device, a compatible read/write capable DDR device, a compatible read/write capable DDR2 device, a compatible read/write capable GDDR device, a compatible read/write capable GDDR2 device, and a compatible read/write capable RDRAM device.

69. The method of claim 60, further comprising:
generating and evaluating ECC data for each data access request.

70. The method of claim 60, further comprising:
managing a DRAM memory array with the internal controller.

71. The method of claim 70, wherein presenting the non-volatile memory device as a synchronous memory device through a synchronous memory interface further comprises selectively presenting the DRAM memory array as a synchronous memory device through a synchronous memory interface.

72. The method of claim 70, wherein presenting the non-volatile memory device as a synchronous memory device through a synchronous memory interface further comprises selectively presenting the DRAM memory array as a synchronous memory device through a synchronous memory interface, where data is selectively copied from the non-volatile memory device and the corresponding addresses remapped to one or more internal addresses of one or more DRAM memory array

sections to operate as "shadow" memory.

73. The method of claim 70, wherein buffering data access requests received through the synchronous memory interface in an internal buffer memory further comprises buffering data access requests received through the synchronous memory interface in the DRAM memory array as an extended read and/or write data buffer memory.

74. The method of claim 70, wherein selectively presenting the DRAM memory array as a synchronous memory device through a synchronous memory interface further comprises selectively presenting the DRAM memory array as a synchronous memory device through a synchronous memory interface, where the DRAM memory array operates as "scratch pad" memory.

75. A method of operating a NAND architecture Flash memory device comprising:
managing the NAND architecture Flash memory device with an internal controller;
presenting the NAND architecture Flash memory device as a synchronous memory device through a synchronous memory interface; and
buffering data access requests received through the synchronous memory interface in an internal buffer memory.

76. The method of claim 75, wherein buffering data access requests received through the synchronous memory interface in an internal buffer memory further comprises buffering read data access requests in the internal buffer memory.

77. The method of claim 75, wherein buffering data access requests received through the synchronous memory interface in an internal buffer memory further comprises changing the status of one of an external "ready/busy" pin and a status register to indicate that the non-volatile memory device is busy.

78. The method of claim 75, wherein buffering data access requests received through the synchronous memory interface in an internal buffer memory further comprises buffering write data access requests in the internal buffer memory.

79. A method of operating a non-volatile memory subsystem comprising:
managing one or more non-volatile memory devices with a controller;
presenting the one or more non-volatile memory devices as a synchronous memory device through a synchronous memory interface; and
buffering data access requests received through the synchronous memory interface in a buffer memory.

80. The method of claim 79, wherein at least one of the one or more non-volatile memory devices is one of a NAND architecture Flash, a NOR architecture Flash, EEPROM, Polymer Memory, Ferroelectric Random Access Memory (FeRAM), Ovionics Unified Memory (OUM), Magnetoresistive Random Access Memory (MRAM), Molecular Memory, and Carbon Nanotube Memory.

81. The method of claim 79, wherein buffering data access requests received through the synchronous memory interface in an internal buffer memory further comprises buffering read data access requests in the internal buffer memory.

82. The method of claim 79, wherein presenting the one or more non-volatile memory devices as a synchronous memory device through a synchronous memory interface further comprises changing the status of one of an external "ready/busy" pin and a status register to indicate that the non-volatile memory device is busy.

83. The method of claim 79, wherein buffering data access requests received through the synchronous memory interface in an internal buffer memory further comprises changing the status of one of an external "ready/busy" pin and a status register to indicate that the non-volatile memory device is busy.

84. The method of claim 79, wherein buffering data access requests received through the synchronous memory interface in an internal buffer memory further comprises buffering write data access requests in the internal buffer memory.

85. The method of claim 84, wherein buffering write data access requests received through the synchronous memory interface in an internal buffer memory further comprises asserting one of an external "busy" pin and a status register to indicate that the buffer memory is full during a write access.

86. The method of claim 79, wherein presenting the one or more non-volatile memory devices as a synchronous memory device through a synchronous memory interface further comprises presenting one of a SDRAM memory device, a DDR memory device, a DDR2 memory device, a GDDR memory device, a GDDR2 memory device, and a RDRAM memory device.

87. The method of claim 86, wherein presenting one of a SDRAM memory device, a DDR memory device, a DDR2 memory device, a GDDR memory device, a GDDR2 memory device, and a RDRAM memory device further comprises presenting as one of a compatible read/write capable SDRAM memory device, a compatible read/write capable DDR memory device, a compatible read/write capable DDR2 memory device, a compatible read/write capable GDDR memory device, a compatible read/write capable GDDR2 memory device, and a compatible read/write capable RDRAM memory device.

88. The method of claim 79, further comprising:
generating and evaluating ECC data for each data access request.

89. The method of claim 79, further comprising:
managing one or more synchronous DRAM memory devices with the controller.

90. The method of claim 89, wherein presenting the one or more non-volatile memory devices as a synchronous memory device through a synchronous memory interface further comprises selectively presenting the one or more synchronous DRAM memory devices as a synchronous memory device through a synchronous memory interface.

91. The method of claim 89, wherein presenting the one or more non-volatile memory devices as a synchronous memory device through a synchronous memory interface further comprises selectively presenting the one or more synchronous DRAM memory devices as a synchronous memory device through a synchronous memory interface, where data is selectively copied from the one or more non-volatile memory devices and the corresponding addresses remapped to one or more internal addresses of the one or more DRAM memory devices to operate as "shadow" memory.

92. The method of claim 89, wherein buffering data access requests received through the synchronous memory interface in an internal buffer memory further comprises buffering data access requests received through the synchronous memory interface in the one or more DRAM memory devices as an extended read and/or write data buffer.

93. The method of claim 89, wherein selectively presenting the one or more DRAM memory devices as a synchronous memory device through a synchronous memory interface further comprises selectively presenting the one or more DRAM memory devices as a synchronous memory device through a synchronous memory interface, where the one or more DRAM memory devices operate as "scratch pad" memory.

94. A machine-usable medium, the machine-usable medium containing a software routine for causing a memory controller to execute a method, wherein the method

comprises:

managing one or more non-volatile memory devices with the memory controller;

presenting one or more non-volatile memory devices as a synchronous memory device through a synchronous memory interface; and

buffering data access requests received through the synchronous memory interface in a buffer memory.

95. The system of claim 94, wherein at least one of the one or more non-volatile memory devices is one of a NAND architecture Flash, a NOR architecture Flash, EEPROM, Polymer Memory, Ferroelectric Random Access Memory (FeRAM), Ovionics Unified Memory (OUM), Magnetoresistive Random Access Memory (MRAM), Molecular Memory, and Carbon Nanotube Memory.

96. A system comprising:

a host; and

one or more non-volatile memory devices coupled to the host, wherein each of the one or more non-volatile memory devices comprises,

a non-volatile memory array;

a buffer memory; and

a synchronous memory interface, wherein the non-volatile memory devices comprises a means for interfacing with, managing, and buffering data access to the non-volatile memory array and comprises a means for presenting the non-volatile memory device as a synchronous memory device through the synchronous memory interface.

97. The system of claim 96, wherein at least one of the one or more non-volatile memory devices is one of a NAND architecture Flash, a NOR architecture Flash, EEPROM, Polymer Memory, Ferroelectric Random Access Memory (FeRAM), Ovionics Unified Memory (OUM), Magnetoresistive Random Access Memory (MRAM), Molecular Memory, and Carbon Nanotube Memory.

98. A NAND architecture Flash memory subsystem comprising:
one or more NAND architecture Flash memory devices;
a buffer memory;
a synchronous memory interface; and
a controller coupled to the one or more NAND architecture Flash memory devices, the buffer memory, and the synchronous memory interface, wherein the controller is adapted to interface to and manage the NAND architecture Flash memory devices and to present the NAND architecture Flash memory devices as a synchronous memory device through the synchronous memory interface.

99. A method of operating a NAND architecture Flash memory subsystem comprising:
managing one or more NAND architecture Flash memory devices with a controller;
presenting the one or more NAND architecture Flash memory devices as a synchronous memory device through a synchronous memory interface; and
buffering data access requests received through the synchronous memory interface in a buffer memory.